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EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

1. This office action, in response to the remarks filed 2/8/2007, is a final office action.

Response to Arguments

2. Applicant's arguments filed 2/8/2007 have been fully considered but they are not persuasive. Applicants states Lee does not disclose a single instruction which specifies a plurality of signal values and a plurality of code segments and performs complex multiplication, addition and storing all within a single clock cycle as claimed. The examiner disagrees. Lee states "each of these single instructions cause data to be extracted from the memory (322), processed and an output provided in the form of a despread signal" (abstract). Lee further discloses, upon receipt of a single instruction, the contents of memory locations containing incoming signal values are read from memory and output to the computational circuit. The PN code values also operate on the incoming signal values to produce despread components (paragraph 0021). Complex multiplication of each single value is conducted (figure 6). Complex addition of the results to provide a despread results is shown in figure 6 and paragraph 0024. The despread results are stored in accumulators 610 and 614 in figure 6. The abstract states "The process is performed in response to the generation of the single instruction in response to the generation of the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing various multiplications, summations and accumulations, all in a single instruction cycle." Lee restates this information in paragraph 0022. Whenever the instruction is executed, the in-band and quadrature components (plurality of signal values) are extracted from the

memory, the corresponding PN code data (plurality of code segments of a despreading code) are extracted from the memory and the process is carried out as described above with reference to figure 6. This all occurs in a single instruction cycle. Therefore, for these reasons and the reasons stated in the previous office action, the rejections of the claims are maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-14 and 16-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (EP 1 017 183 A2).

Regarding claims 1 and 8, Lee discloses a method for the despreading of spread spectrum signals in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing various multiplications, summations and accumulations, all in a single instruction cycle (abstract). The despreading operation of the spread spectrum RAKE receiver consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claims 2 and 9, the method further includes including a previous result from a previous instruction in the complex addition which provides the despread result (paragraph 0009).

Regarding claims 3 and 10, the spreading factor is disclosed in paragraph 0005.

Regarding claims 4, 5, 11 and 12, the PN sequence is a sequence of +1 and –1 for the I and Q components (paragraph 0007).

Regarding claims 6, 7, 13 and 14, the incoming signal is stored in buffers of size N. the signal comprises real and imaginary bits (paragraph 0016).

Regarding claim 16, Lee discloses a digital signal processor shown in figure 1. The processor includes a memory 322, instruction generator 316, in path processor block 310 and numerous process blocks 320. The digital signal processor executes a method for the despreading of spread spectrum signals in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing various multiplications, summations and accumulations, all in a single instruction cycle (abstract). The despreading operation of the spread spectrum RAKE receiver consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claim 17, the spreading factor is disclosed in paragraph 0005.

Regarding claims 18 and 19, the PN sequence is a sequence of +1 and –1 for the I and Q components (paragraph 0007).

Regarding claims 20 and 21, the incoming signal is stored in buffers of size N. the signal comprises real and imaginary bits (paragraph 0016).

Regarding claim 22, Lee discloses a method for calculating output data in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing various multiplications, summations and accumulations, all in a single instruction cycle (abstract). The operation of the DSP consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claim 23, the PN sequence is a sequence of +1 and –1 for the I and Q components (paragraph 0007).

Regarding claims 24 and 25, the method despreads an incoming signal (abstract).

Regarding claim 26, the received signal is a spread spectrum/CDMA signal (abstract).

Regarding claim 27, Lee discloses a method for calculating output data in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing multiplication in a single instruction cycle (abstract). The operation of the DSP consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claim 28, Lee discloses a method for calculating output data in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing various multiplications, summations and accumulations, all in a single instruction cycle (abstract). The operation of the DSP consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claim 29, the incoming signal is stored in buffers of size N. the signal comprises real and imaginary bits (paragraph 0016).

Regarding claim 30, the PN sequence is a sequence of +1 and –1 for the I and Q components (paragraph 0007).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kevin M. Burd
3/21/2007

KEVIN BURD
PRIMARY EXAMINER